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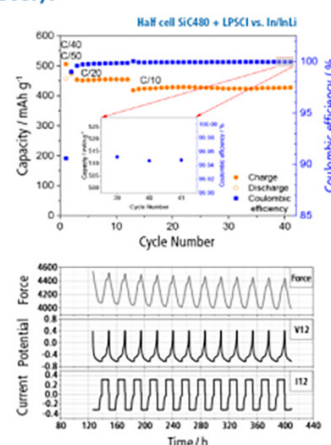
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Characteristics of β -Ga₂O₃/Al₂O₃/Pt Capacitors with a Ga₂O₃ Surface Modified Using the Dummy-SiO₂ Process

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The characteristics of β -Ga₂O₃/Al₂O₃/Pt capacitors fabricated via the dummy-SiO₂ (*d*-SiO₂) process at 800 °C under O₂ (D-O₂), N₂ (D-N₂), and 3% H₂ (D-H₂) atmospheres were investigated. The surface of Ga₂O₃ after the *d*-SiO₂ process was as smooth as that after the sulfuric acid-hydrogen peroxide mixture treatment (Control). The flatband voltage (V_{fb}) hysteresis decreased as follows: Control (0.76 V) > D-H₂ (0.56 V) > D-N₂ (0.43 V) > D-O₂ (0.37 V). The interface state density of the D-O₂ capacitor was significantly reduced to $6 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ at -0.4 eV from conduction band. The V_{fb} shift caused by the electron traps according to the near-interface trap model under positive bias stress substantially improved for the capacitors fabricated by the *d*-SiO₂ process. The poor characteristics of the Control capacitor are due to the presence of the unstable layer on the Ga₂O₃ surface. The improved electrical characteristic of the *d*-SiO₂ capacitors is due to the modified Ga₂O₃ surface, which eliminated the unstable Ga₂O₃ layer. This is the result of hydrogen contained within the dummy SiO₂ layer supporting the removal of Ga₂O₃. The difference in the decomposition reaction of Ga₂O₃ due to the atmosphere gas of the *d*-SiO₂ process leads to differences in electrical properties. © 2026 The Author(s). Published on behalf of The Electrochemical Society by IOP Publishing Limited. This is an open access article distributed under the terms of the Creative Commons Attribution 4.0 License (CC BY, <https://creativecommons.org/licenses/by/4.0/>), which permits unrestricted reuse of the work in any medium, provided the original work is properly cited. [DOI: 10.1149/2162-8777/ae7ac0]



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The most stable gallium oxide (Ga₂O₃) phase, β -Ga₂O₃, is an ultra-wide-bandgap semiconductor for next-generation high-power transistors. β -Ga₂O₃ metal-oxide-semiconductor field-effect transistors (MOSFETs)^{1,2} have been widely investigated because β -Ga₂O₃ has a large bandgap of 4.9 eV³⁻⁵ and a high breakdown electric field of 8 MV cm⁻¹.¹ In addition, large single-crystal β -Ga₂O₃ wafers can be fabricated by melt growth methods including the floating zone⁶ and Czochralski techniques⁷ as well as edge-defined film-fed growth,^{8,9} which gives β -Ga₂O₃ an economic advantage over GaN and SiC.

For MOSFETs, various materials such as SiO₂,^{2,10-14} Al₂O₃,¹⁵⁻²⁰ HfO₂,²¹⁻²⁵ and Al₂O₃/HfO₂ bilayers²⁶ have been investigated as gate insulators. Among these, Al₂O₃ is considered a promising candidate material for low-temperature fabrication processes, whereas SiO₂ is considered a candidate material for high-temperature fabrication processes. Understanding the characteristics of the β -Ga₂O₃/insulator interface for β -Ga₂O₃ MOSFETs is important. An abnormal flatband voltage (V_{fb}) shift and V_{fb} hysteresis occur in β -Ga₂O₃/insulator MOS capacitors because the insulator and an unstable layer on the β -Ga₂O₃ surface had oxygen vacancies (V_o) and electrical defects.^{12-14,16,27} To reduce the concentration of these electrical defects, researchers have investigated the effects of post-deposition annealing (PDA) and post-metallization annealing (PMA).^{17,20} PDA at temperatures as high as 1000 °C under an N₂ and/or O₂ atmosphere have been reported to reduce the density of interface traps (D_{it}) at the Ga₂O₃/SiO₂ interface.^{13,14} For β -Ga₂O₃/Al₂O₃ MOS capacitors, the β -Ga₂O₃/Al₂O₃ interface was improved by either PDA at 500 °C²⁰ or by PMA at 500 °C.¹⁷ We have previously reported that the combination of PDA and PMA at 300 °C substantially reduced the fixed charge and D_{it} at the β -Ga₂O₃/Al₂O₃ interface.^{28,29} PDA was observed to result in the diffusion of Ga from the Ga₂O₃ substrate into the Al₂O₃ insulator. This diffusion may affect the electrical properties of the Al₂O₃ insulator. Therefore, it is important to improve the properties of the Ga₂O₃/insulator without using PDA.

Wet processes at temperatures less than 200 °C have generally been used to clean Ga₂O₃ surfaces; however, these cleaning processes have not always been effective. Other effective processes for modifying the Ga₂O₃ surface are required. We previously reported that using a dummy-SiO₂ (*d*-SiO₂) process can modify the GaN substrate with epi-like grown unstable GaO_x surface, resulting in improved electrical properties.^{30,31} After modification to remove unstable GaO_x and form stable GaO_x on the GaN surface via a

d-SiO₂ process, we fabricated an Al₂O₃ insulator and Pt gate electrode at a low temperature (300 °C), thereby suppressing reactions at the GaN/modified GaO_x/Al₂O₃ interface. We also observed by scanning transmission electron microscopy with energy-dispersive X-ray spectroscopy (STEM-EDS) analysis that oxygen-oriented stable Ga₂O₃ formed on the GaN surface fabricated by a *d*-SiO₂ process.³² The *d*-SiO₂ process is also considered effectively for modifying the unstable Ga₂O₃ layer of Ga₂O₃ surface.

In the present study, we modified from the unstable layer which had some electrical defects to stable layer on the β -Ga₂O₃ surface using a *d*-SiO₂ process under various atmospheres and investigated the effect of the process on the electrical properties of β -Ga₂O₃/Al₂O₃/Pt MOS capacitors.

Experimental

Figure 1 shows the β -Ga₂O₃/Al₂O₃/Pt MOS capacitor fabrication flow using a *d*-SiO₂ process. Initially, n⁺- β -Ga₂O₃ ($3.7 \times 10^{18} \text{ cm}^{-3}$) (001) substrates with a 5 μm -thick Si-doped n- β -Ga₂O₃ epilayer ($2.0 \times 10^{16} \text{ cm}^{-3}$) were cleaned with a sulfuric acid–peroxide mixture (SPM) (H₂SO₄:H₂O₂ = 1:1) to remove organic residues. Four different processes were applied to the samples in parallel. In the *d*-SiO₂ process, a 5 nm-thick SiO₂ layer was deposited onto β -Ga₂O₃ substrates via plasma-enhanced atomic layer deposition (PE-ALD) at 300 °C using tris(dimethylamino) silane as a precursor and O₂ as the plasma gas. PDA was carried out at 800 °C for 300 s under O₂, N₂, and 3% H₂ atmospheres in a rapid thermal annealing system; the resultant samples are referred to as D-O₂, D-N₂, and D-H₂, respectively. With an etching rate of 0.55 nm s⁻¹, the SiO₂ layer was removed in 20 s using buffered HF (BHF) solution. Immediately after these four procedures, a 10 nm-thick Al₂O₃ film was deposited as a gate insulator onto the β -Ga₂O₃ via ALD at 300 °C using trimethylaluminum (TMA) as a precursor and H₂O gas. Finally, to fabricate MOS capacitors, a 100 nm-thick Pt gate electrode was deposited onto the Al₂O₃ insulator through a shadow mask (~100 μm in diameter) via electron beam evaporation; a Ti (20 nm)/Pt (100 nm) ohmic contact was subsequently deposited onto the backside of the n⁺- β -Ga₂O₃ substrates. PMA was carried out at 300 °C for 300 s under a N₂ atmosphere. As reference, a β -Ga₂O₃/Al₂O₃/Pt MOS capacitor was prepared without the *d*-SiO₂ process; this capacitor is referred to as “Control.” To study cleaning method on β -Ga₂O₃ surface, β -Ga₂O₃/Al₂O₃(30 nm)/Pt capacitors after SPM and BHF treatments were also prepared. A 18 nm-thick SiO₂ film was deposited onto the β -Ga₂O₃ substrate via PE-ALD at

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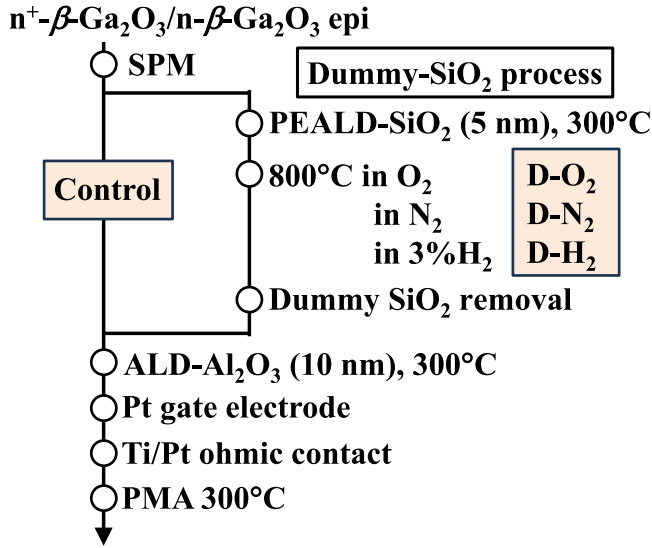


Figure 1. β -Ga₂O₃/Al₂O₃/Pt MOS capacitor fabrication flow using d -SiO₂ process.

300 °C to evaluate the Ga and H concentrations in the SiO₂ layer after PDA.

For the fabricated β -Ga₂O₃/Al₂O₃/Pt MOS capacitors, capacitance–voltage (C – V) measurements were performed at room temperature with a frequency of 1 MHz under dark conditions using an Agilent B 1500 A semiconductor device parameter analyzer. The gate bias was swept from the depletion to the accumulation region and back to the depletion region. The number of repeat voltage sweeps was five. The V_{fb} value for each specimen was estimated from the C – V data using the MIRAI-ACCEPT software,³³ which is a C – V simulation program that considers surface potential and oxide voltage. The D_{it} was estimated using a conductance method.³⁴ An equivalent parallel conductance (G_p/ω) in depletion bias condition is calculated, where ω is frequency. The frequency varied from 1 kHz to 1 MHz while the $V - V_{fb}$ voltage applied 1.0 V.^{28,29} Positive-bias stress (PBS) tests were conducted at room temperature for a stress time of 300 s by systematically varying the bias $V - V_{fb}$ from 2.0 to 4.0 V. After stress times of 1, 10, 50, 100, 150, 250, and 300 s, the C – V characteristics were repeatedly measured. The direction of voltage sweeping for the C – V measurements after PBS was from accumulation to depletion to avoid electron emission from traps. In addition, the surfaces of the Ga₂O₃ substrates after sulfuric acid-hydrogen peroxide mixture (SPM) cleaning treatment and the d -SiO₂ process were characterized by atomic force microscopy (AFM) before an Al₂O₃ insulator was deposited. The Ga and H depth profiles in the SiO₂ films were evaluated using secondary-ion mass spectrometry (SIMS).

Results

We used AFM to evaluate the surface of the Ga₂O₃ substrates after the SPM treatment and the d -SiO₂ process (Fig. 2). The root mean square (RMS) surface roughness of the SPM-treated specimen was 0.24 nm over a $1.0 \times 1.0 \mu\text{m}^2$ field of view. The RMS of the sample subjected to d -SiO₂ was 0.25 nm, suggesting that the d -SiO₂ process did not lead to increased surface roughness. After the d -SiO₂ process, no Si diffusion occurred into Ga₂O₃ via analysis of the SIMS Si depth profile and XPS Ga_{3d} spectra (results not shown). To establish a cleaning method for β -Ga₂O₃ surfaces, SPM and BHF treatment after SPM were performed. Figure 3 shows V_{fb} hysteresis and RMS-RMS(SPM) values as a function of the BHF treatment time. The etching rate of the β -Ga₂O₃ substrate found to be 0.03 nm min^{-1} using BHF solution. RMS value after BHF treatment at 1 min significantly increased by 0.25 nm compared to the SPM and maintained same value, thereafter, indicating that surface

roughness of the β -Ga₂O₃ substrate increased using BHF solution. Furthermore, the increase of the surface roughness caused a large V_{fb} hysteresis of 0.23 V in the capacitor with BHF treatment at 1 min compared to that (0.08 V) of SPM treatment. The V_{fb} hysteresis increased as the BHF treatment time increased. As a result, the SPM treatment was employed as the surface cleaning method. Figure 4 shows the C – V characteristics of the Control, D-O₂, D-N₂, and D-H₂ β -Ga₂O₃/Al₂O₃/Pt MOS capacitors. For these capacitors, no frequency dispersion was observed in the depletion region at low measurement frequencies (1–10 kHz, results not shown). In the first voltage sweep after capacitor fabrication, all capacitors showed a positive clockwise C – V hysteresis. In the second measurement from the depletion to the accumulation region, the C – V curve shifted toward the positive direction for all of the capacitors. Figure 4e shows the V_{fb} hysteresis as a function of the number of voltage sweeps. At the first voltage sweep, the V_{fb} hysteresis for the Control, D-H₂, D-N₂, and D-O₂ capacitors were 0.7, 0.56, 0.42, and 0.39 V, respectively. The V_{fb} hysteresis drastically decreased at the second voltage sweep and reached its minimum value at the third voltage sweep. These results indicate the presence of electron trap sites and suggest that electrons were trapped in these sites during the first voltage sweep from the depletion to the accumulation region. The minimum V_{fb} hysteresis for the Control, D-H₂, D-N₂, and D-O₂ capacitors were 0.12, 0.11, 0.09, and 0.08 V, respectively, at five voltage sweeps. We carried out C – V measurements with various $V - V_{fb}$ voltage amplitudes of 1.2–4.0 V at 1 MHz. Note that the maximum applied $V - V_{fb}$ corresponds to 4 MV cm^{-1} . Figure 5 shows the V_{fb} hysteresis as a function of the applied $V - V_{fb}$ at the first voltage sweep. For all of the capacitors, the V_{fb} hysteresis increased when $V - V_{fb}$ increased. The increase in V_{fb} hysteresis for $V - V_{fb}$ greater than 2 V is similar to that for GaN/Al₂O₃ MOS capacitors prepared by the d -SiO₂ process.³⁰ In particular, the Control capacitor exhibited a larger V_{fb} hysteresis than the capacitors prepared using the d -SiO₂ process under various atmospheres, and the maximum V_{fb} hysteresis reached 0.76 V. These results suggest that the trap/detrap sites must be formed at the Ga₂O₃/Al₂O₃ interface. However, the V_{fb} hysteresis for the d -SiO₂-processed capacitors decreased as follows: D-H₂ (0.56 V) > D-N₂ (0.43 V) > D-O₂ (0.37 V). These results indicate that the density of the trap/detrap sites at the Ga₂O₃/Al₂O₃ interface decreased because of the modification of the Ga₂O₃ surface by the d -SiO₂ process. To understand the characteristics of the Ga₂O₃/Al₂O₃ interfaces, the D_{it} was estimated using a conductance method.³⁴ The energy distribution of D_{it} for the Control, D-O₂, D-N₂, and D-H₂ capacitors are shown in Fig. 6. The Control capacitor exhibited a high D_{it} of above $10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ at the energy level of $E_c - E = 0.4 \text{ eV}$, where E_c is the energy level of the conduction band minimum. In contrast, The D-N₂ and D-H₂ capacitors showed small, very similar D_{it} profiles. The D-O₂ capacitor significantly reduced D_{it} value as low as $6 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ at $E_c - E = 0.4 \text{ eV}$. The effect of atmosphere gas on electrical properties will be discussed later.

We next compared the V_{fb} shifts for the four kinds of capacitors under PBS conditions. Figure 7 shows the V_{fb} shifts for the Control, D-O₂, D-N₂, and D-H₂ capacitors as a function of stress time under various bias $V - V_{fb}$ of 2.0–4.0 V. A stronger applied bias voltage and longer stress time resulted in a larger V_{fb} shift for all of the capacitors, indicating that the time constant and energy depth for traps are diversified. The Control capacitor exhibited a larger V_{fb} shift than the capacitors prepared using the d -SiO₂ process with any atmospheres. The maximum V_{fb} shift for the Control, D-H₂, D-N₂, and D-O₂ samples was 1.26, 1.05, 0.86, and 0.81 V, respectively, when the bias voltage was 4.0 V and the stress time was 300 s. Notably, the d -SiO₂ process effectively reduced the V_{fb} shift induced by a high bias voltage stress. The same trend observed in Fig. 5 is seen in Fig. 8. The poor electrical characteristics of the Control capacitor suggest the presence of an unstable layer on the Ga₂O₃ surface. In addition, the V_{fb} shift exhibits a linear relationship with stress time on a logarithmic scale, which can be explained by electron trapping by the near-interface traps close to the

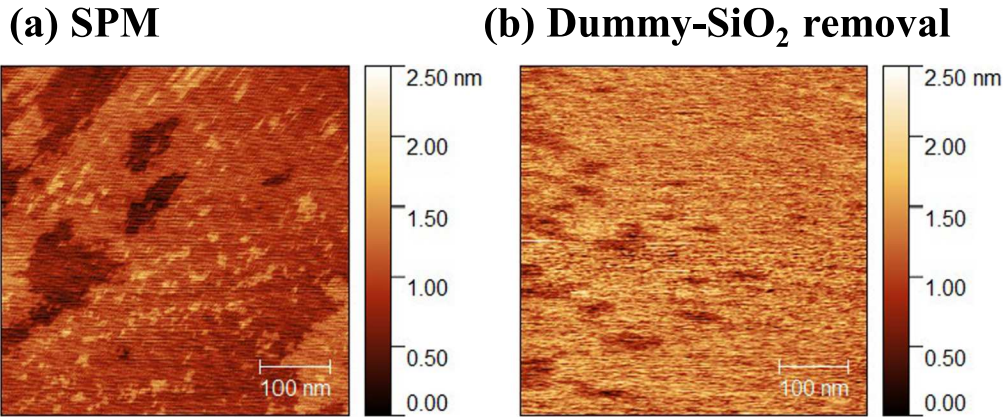


Figure 2. AFM images of Ga₂O₃ surfaces after (a) SPM treatment and (b) the dummy-SiO₂ removal.

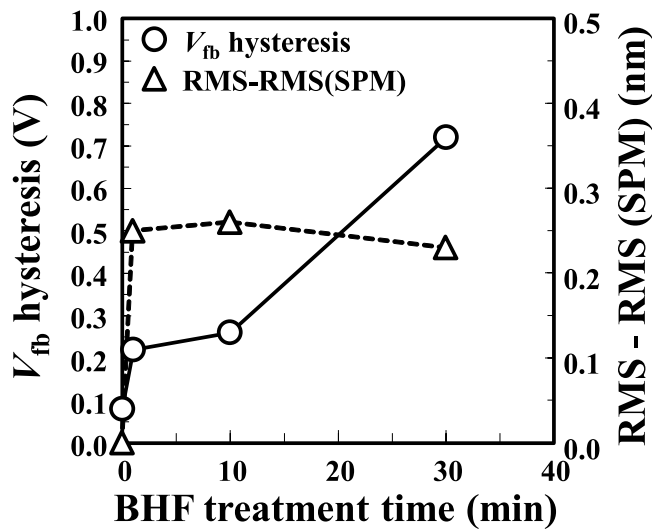


Figure 3. V_{fb} hysteresis and RMS-RMS(SPM) value as a function of the BHF treatment time.

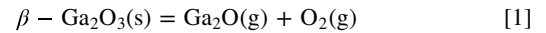
Ga₂O₃/Al₂O₃ interface. The same phenomenon in GaN/SiO₂ stacks is also explained by this model.³⁶ According to this model, injected electrons are trapped at the trap sites nearest to the interface. Once those sites are full, the electrons are trapped at the next-nearest trap sites.

Discussion

We found that the *d*-SiO₂ process effectively improves the characteristics of β -Ga₂O₃/Al₂O₃/Pt MOS capacitors. Regarding electrical properties, an approximately half- V_{fb} hysteresis and an approximately 0.45 V smaller V_{fb} shift under PBS were found for the β -Ga₂O₃/Al₂O₃/Pt MOS capacitor fabricated using the *d*-SiO₂ process in O₂ compared with those observed for the Control capacitor. This hysteresis and smaller shift were attributed to the modification of the Ga₂O₃ surface by the *d*-SiO₂ process. To clarify this modification of the Ga₂O₃ surface during the *d*-SiO₂ process under various atmospheres, we evaluated the Ga depth profile in the SiO₂ layers using SIMS analysis. Figure 9 shows depth profiles of the Ga concentration in Ga₂O₃/SiO₂ stacks annealed at 800 °C under O₂, N₂, and 3% H₂ atmospheres. In this figure, as-grown refers to a specimen not subjected to annealing. Compared with the Ga concentration in the as-grown specimen, those in the SiO₂ layers annealed at 800 °C increased, irrespective of the atmosphere. In particular, the Ga concentration in the specimen annealed under H₂ gas increased by more than two orders of magnitude compared with

that in the as-grown specimen. In the specimens annealed under O₂ and N₂ atmospheres, the Ga concentration increased by approximately one order of magnitude, and that in the specimen annealed under N₂ was slightly greater than that in the specimen annealed under O₂. The Ga concentration correlates with the amount of Ga₂O₃ decomposition, and Ga₂O₃ decomposition increases as follows: D-H₂ » D-N₂ > D-O₂.

We investigated the effect of the atmosphere gas on the decomposition of β -Ga₂O₃. The decomposition of β -Ga₂O₃ under N₂ gas (Eq. 1) has been reported to start at 1150 °C.^{35,37}

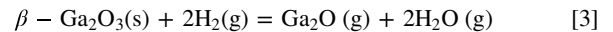


In addition, Ga₂O has been reported to be further decomposed according to Eq. 2 at approximately the same temperature:^{35,36}



Therefore, these decomposition reactions cannot proceed at 800 °C.

By contrast, in N₂ + H₂ mixture gas, the onset of decomposition of β -Ga₂O₃ (Eq. 3) has been reported to be lowered to 350 °C and the decomposition rate has been reported to increase as the annealing temperature is increased from 350 to 600 °C.³⁶



These previous reports indicate that, in the present study, the decomposition of Ga₂O₃ proceeded, resulting in modification of the Ga₂O₃ surface.

To understand the increase in the Ga concentration in the SiO₂ layers under N₂ and O₂ atmospheres, we used SIMS to evaluate the hydrogen concentration in SiO₂ films fabricated by PE-ALD. Figure 10 shows depth profiles of the hydrogen concentration in Ga₂O₃/SiO₂ stacks annealed at 900 °C under O₂ and N₂ atmospheres. The hydrogen concentration in the as-grown SiO₂ film was found to be as high as 4×10^{21} atoms cm⁻³. The hydrogen concentration decreased to 4×10^{20} atoms cm⁻³ after the films were annealed at 900 °C, irrespective of whether an O₂ or N₂ gas atmosphere was used, indicating that approximately 3.6×10^{21} atoms cm⁻³ of hydrogen was released from the SiO₂ layer when the films were annealed at 900 °C. Although the *d*-SiO₂ process was conducted at a slightly lower temperature of 800 °C, assuming that it releases a comparable amount of H₂ gas, Ga₂O₃ decomposition according to Eq. 3 occurred even under an N₂ or O₂ gas atmosphere. In the *d*-SiO₂ process under N₂ or O₂ gas, an extremely thin layer on the Ga₂O₃ surface could be removed because Ga₂O₃ decomposition stopped when hydrogen atoms release from the SiO₂ dummy layer is completed. Here, it is thought that the Ga₂O₃ surface has not been

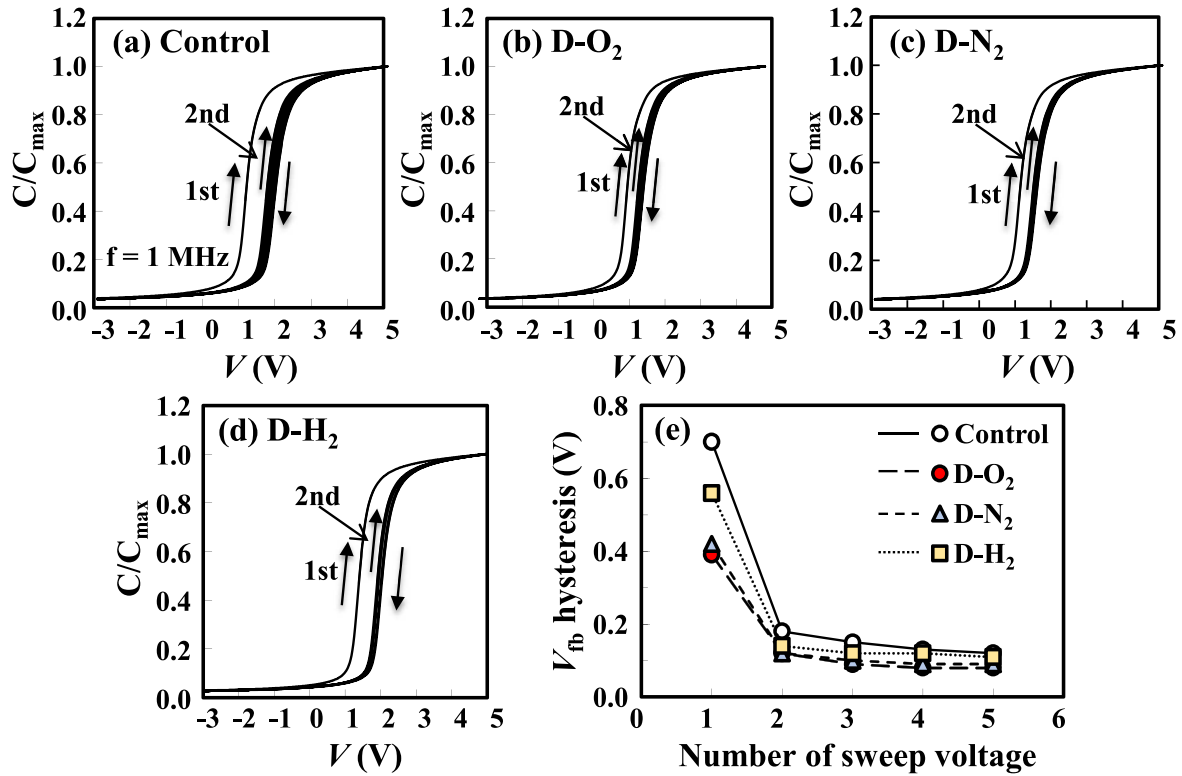


Figure 4. C - V characteristics of the (a) Control, (b) D-O₂, (c) D-N₂, and (d) D-H₂ capacitors. In (a)–(d), the number of voltage sweeps was five. (e) V_{fb} hysteresis as a function of number of voltage sweeps.

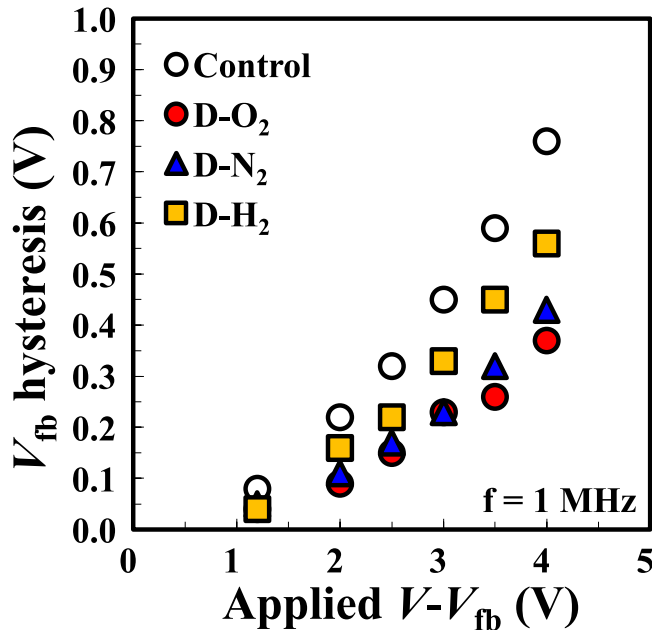


Figure 5. V_{fb} hysteresis as a function of applied $V - V_{fb}$ at first voltage sweep for the Control, D-O₂, D-N₂, and D-H₂ capacitors.

completely decomposed, and that V_o and Ga vacancies have partially formed on the surface. Although oxygen atoms from the SiO₂ film have been supplied since the early stages of annealing,³⁸ oxidation dominantly occurs after hydrogen atoms released. As a result, oxygen atoms from SiO₂ film are thought to compensate for V_o sites and decrease electrical defects. In particular, O₂ gas enabled the

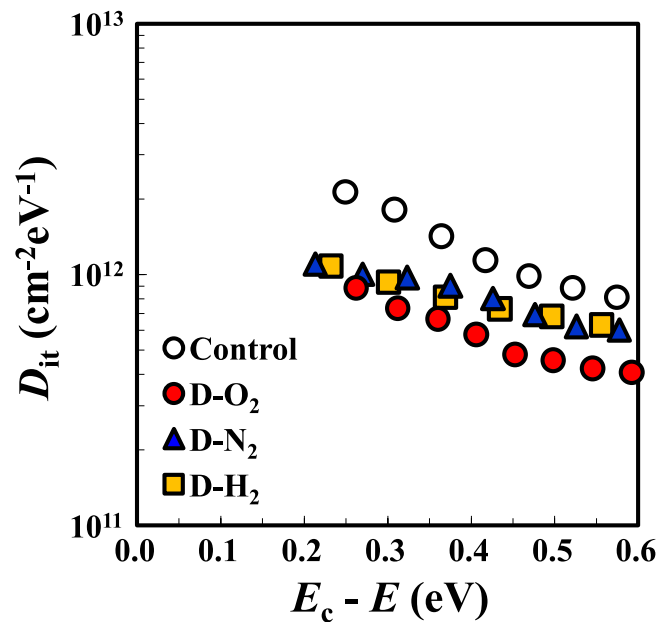


Figure 6. D_{it} distributions for the Control, D-O₂, D-N₂ and D-H₂ capacitors.

removal of the thinnest Ga₂O₃ surface layer because oxygen atoms from outside partially inhibits the decomposition of Ga₂O₃ by H₂ gas in Eq. 3 and compensate for V_o sites. Considering with Ga depth profile in Fig. 9, as a result, the unstable layer on the Ga₂O₃ surface was effectively removed and a modified Ga₂O₃ surface was obtained. However, in the d -SiO₂ process under H₂ gas, since hydrogen atoms are constantly supplied from outside, Eq. 3 proceeded. Excess Ga₂O₃

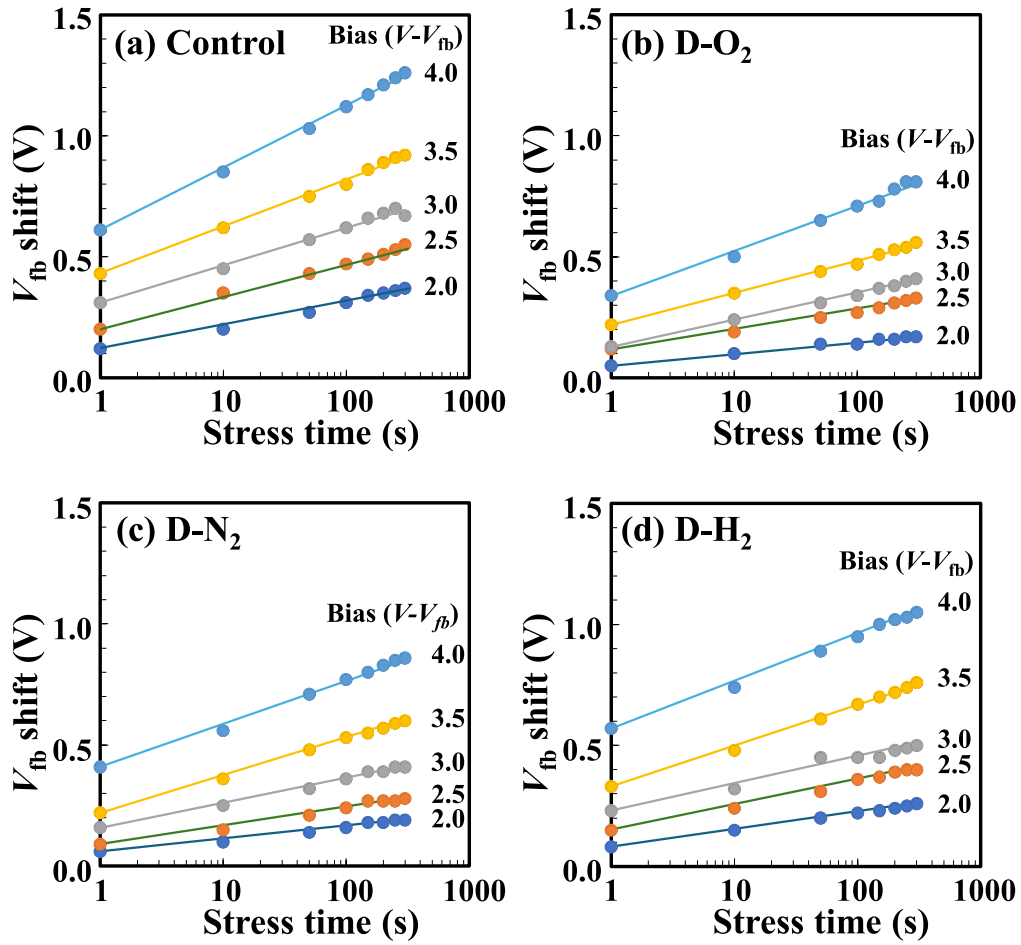


Figure 7. V_{fb} shifts at measurement frequency of 1 MHz as a function of stress time under positive-bias stress conditions for the (a) Control, (b) D-O₂, (c) D-N₂, and (d) D-H₂ capacitors. Various bias voltages, $V - V_{fb}$, ranging from 2.0 to 4.0 V were applied.

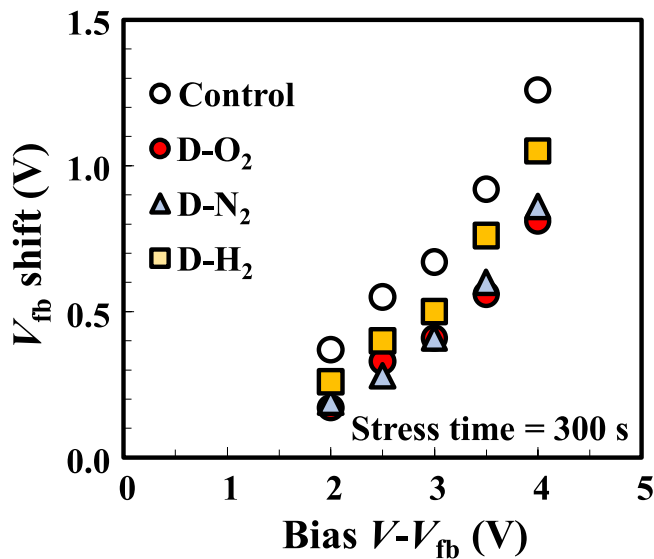


Figure 8. V_{fb} shifts as a function of bias voltage, $V - V_{fb}$, for the Control, D-O₂, D-N₂, and D-H₂ capacitors. The stress time was 300 s.

removal from the Ga₂O₃ surface caused and V_o remained on the Ga₂O₃ surface because of no oxygen supply. As a result, these V_o led to a degradation of the electrical properties. To enhance the effect of the *d-SiO₂* process, further research is needed to optimize parameter such as annealing duration time and atmosphere.

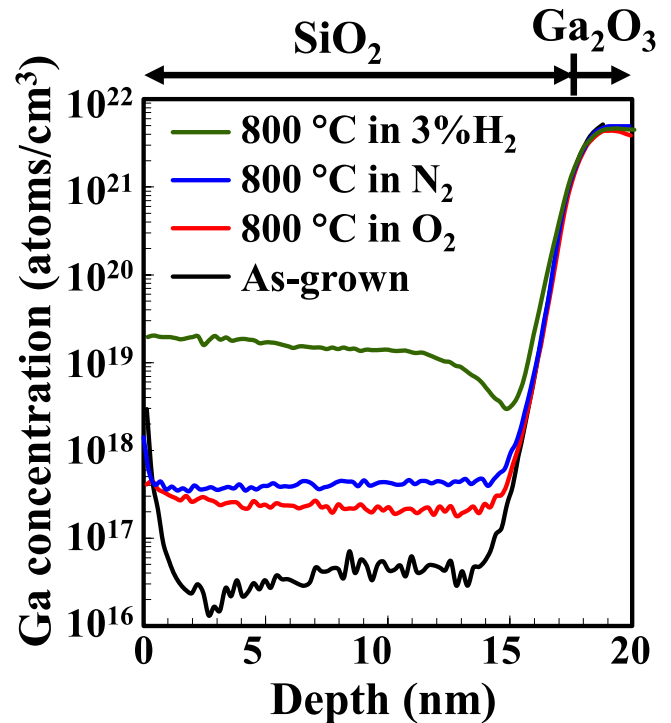


Figure 9. Ga depth profile in Ga₂O₃/SiO₂ stacks subjected to various PDA treatments at 800 °C under O₂, N₂, and 3% H₂ atmospheres, along with profile for an as-grown sample, as determined by SIMS measurements.

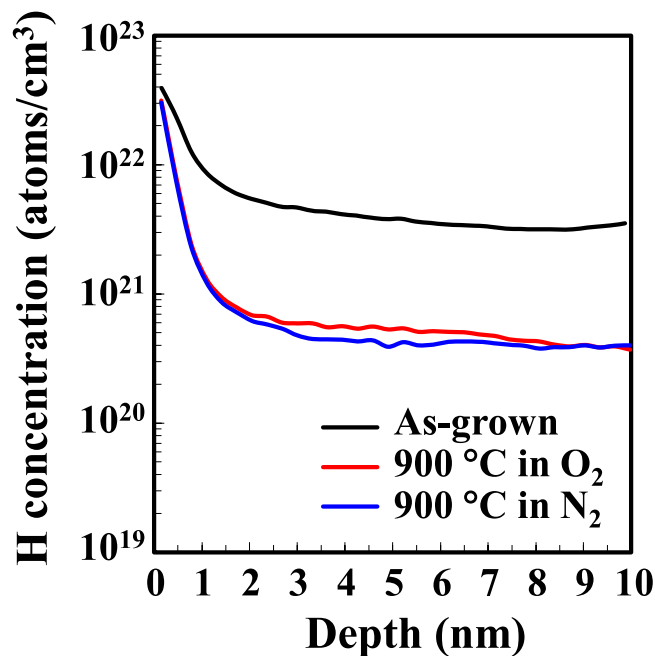


Figure 10. Hydrogen depth profiles in $\text{Ga}_2\text{O}_3/\text{SiO}_2$ stacks subjected to various PDA treatments at 900°C under O_2 and N_2 atmospheres, along with profile for an as-grown sample, as determined by SIMS measurements.

Conclusions

Using a proposed Ga_2O_3 surface treatment—the $d\text{-SiO}_2$ process under O_2 , N_2 , and 3% H_2 atmospheres—we systematically investigated the electrical properties of $\beta\text{-Ga}_2\text{O}_3/\text{Al}_2\text{O}_3/\text{Pt}$ MOS capacitors. The $d\text{-SiO}_2$ capacitors were found to exhibit improved V_{fb} hysteresis and V_{fb} stability under PBS compared with a capacitor that has an unstable layer without the $d\text{-SiO}_2$ process. In the $d\text{-SiO}_2$ process, residual hydrogen that remained in the SiO_2 dummy layer removed the unstable surface layer of Ga_2O_3 even when the specimens were annealed at a low temperature of 800°C , resulting in superior electrical characteristics.

Acknowledgments

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